TECHNOLOGICAL FOUNDATIONS AND FUTURE DIRECTIONS OF LARGE-SCALE INTEGRATED ELECTRONICS

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INTRODUCTION

The technological base of the electronics industry has undergone dramatic change in the past 20 years, largely related to the expansion of the use of materials technology. With the invention of the transistor in 1948, semiconductor materials processing provided the technology for an entirely new class of electronic devices. The invention of the monolithic integrated circuit in 1958 extended the use of materials technology to the formation of complete circuit functions on chips of semiconductor. We are now entering another phase of the expansion of materials technology, in which complete equipment components will be processed on slices of semiconductor.

It is the purpose of this paper to discuss the technological foundations and future directions of this latter phase.

This phase has already been given several names, some of which are "large-scale integration" (LSI), "computer on a slice," and "array technology." The term "large-scale integration" is close to being the most descriptive, although at times the syntax is awkward. A somewhat more precise term is "large-scale integrated electronics." We will use LSI to abbreviate both "large-scale integrated electronics" and "large-scale integration."

The products of large scale integrated electronics will be called Integrated Equipment Components (IEC's) to distinguish from integration to the circuit function (Integrated Circuits, IC's).

In order to set the stage for the discussion of large-scale integrated electronics technology, Fig. 1 is included for review of the technologies of discrete semiconductor devices and monolithic integrated circuits. The reader is referred to the December 1964 issue of *Proceedings of IEEE* [1] for a comprehensive review of integrated electronics. The article by Jay Lathrop [2] is an excellent discussion of integrated circuits technology. A discussion of the history of semiconductor technology is contained in Ref. 3, and the status of large-scale integration technology in 1965 is reviewed in Ref. 4. Recent published reports of meetings concerning LSI are listed in Ref. 5.

An important conclusion of Fig. 1 is that there are potentially 40,000 gates per 1-inch slice of silicon. The use of a 1″ slice of silicon is arbitrary—the industry is moving to larger slices. Today 1¼″ is widely used and 3″ diameter is forecast by 1976. A principal goal of LSI technology will be to utilize this logical power in slice form; that is, interconnect the gates such that powerful logic and memory functions are formed on single slices of semiconductor material.

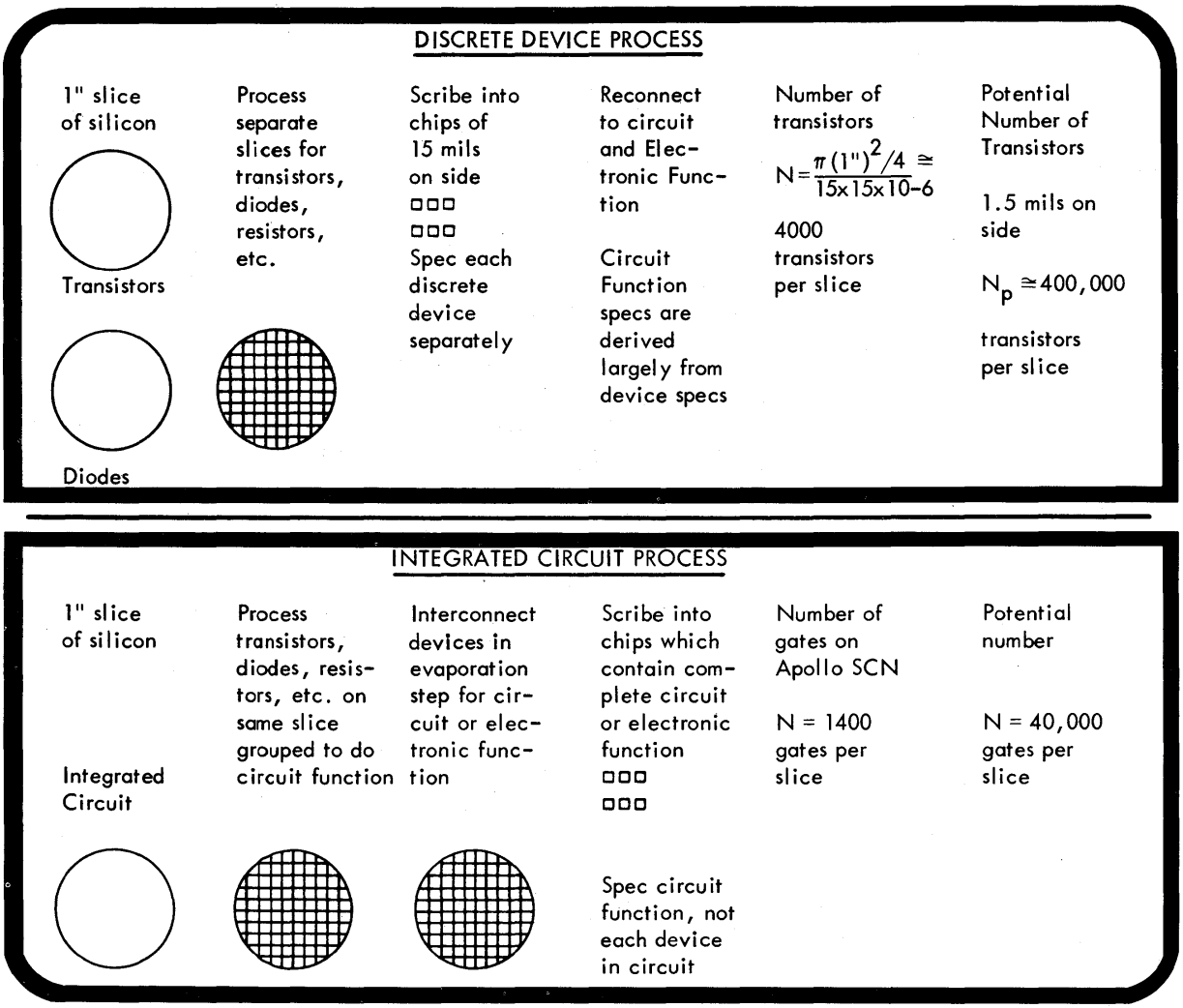


Figure 1. Discrete device and integrated circuit processes.

Interconnections Required to Construct Equipment Components

Before going further in our discussion of the technological foundations of large-scale integrated electronics, let us discuss the problem of building an equipment component, such as a memory or central processor unit, requiring the logical power of, for example, 10,000 gates.

In Fig. 2 it is shown that the construction of an equipment component of 10 K gates from discrete devices requires about 150 K mechanical connections. We have assumed each gate has 10 internal and 5 external connections. Since each gate is connected to something else, a linear slope brings us to 150 K for an equipment component of logical power of 10 K gates.

For multifunction integrated circuits, the 10 mechanical connections needed to interconnect the discrete devices to form gates are made by materials processing (evaporation of metal). Thus a single gate has five terminal connections, and 50 K mechanical connections must be made to achieve an equipment component complexity of 10 K gates (Fig. 2).

We thus conclude that while integration to the circuit function level of complexity has reduced the mechanical interconnection problem (from 150 K to 50 K in this example), there are still a great many mechanical interconnections to be made in order to construct an equipment component.

It is of interest to observe that the use of equipment components as black boxes requires orders of magnitude less external connections, that is, most

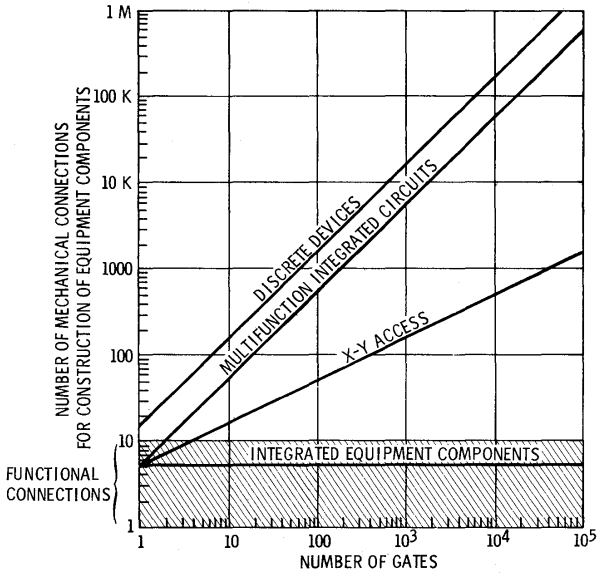


Figure 2. Number of mechanical connections for equipment components vs number of gates.

of the 50 K connections are internal. In Fig. 3, bottom left hand corner, it is shown that a typical ALU of a computer requires 85 external connections to add two 25-bit words.

Defining R as the number of functional connections per bit of processed data,

$$R = \frac{85}{25} = 3.4$$

We note that the other equipment components shown in Fig. 3 have R values in the range of 1–10, relatively independent of the number of gates per equipment component. The shaded area on Fig. 2 will contain the number of functional connections per bit for equipment components. Comparison of the shaded region with the lines for discrete devices and multifunction integrated circuits shows that most of the mechanical connections are internal. Essentially all connections above the shaded area are internal.

As will be developed in detail below, a principal goal of large-scale integration technology is to make these internal connections a part of the materials processing technology (e.g., by evaporation).

Those equipment components in which most of the internal connections are made by materials processing technology we shall call Integrated Equipment Components (IEC's), to distinguish them from Integrated Circuits (IC's) and from equipment components fabricated principally by mechanical techniques. Figure 4 illustrates these definitions qualitatively.

Technologies Suitable for Integrated Equipment Components

The essential requirements of a basic technology are two:

1. It must be capable of forming thousands or more of both active and passive devices in or on a common substrate.
2. It must be capable of interconnecting thousands of active and passive devices into IEC's by a materials process such as evaporation without separate mechanical handling of devices.

Clearly monolithic semiconductor integrated circuit technology has the potential of meeting both of these requirements as shown in Figs. 1 and 4. This paper will be concerned principally with semiconductor technology, but before developing this further, let us consider what other technologies may also be suitable for large-scale integrated electronics. The consideration that the technology must be capable of forming complete electronic functions without intermediate steps of dicing and mechanical handling eliminates the hybrid technologies as we know them today (e.g., thick or thin films, with chip transistors). However, hybrid and discrete device technology, in combination with monolithic semiconductor technology, will add to the flexibility of LSI.

Technologies in addition to silicon that appear to have promise include: thin films, where the TFT

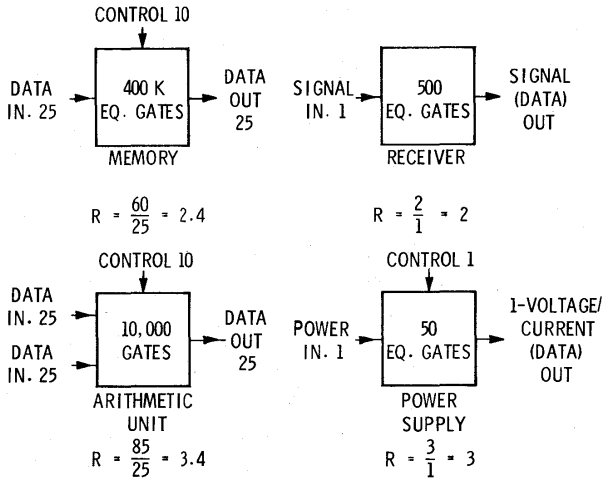


Figure 3. Ratio of functional connections to bits of output data for equipment components.

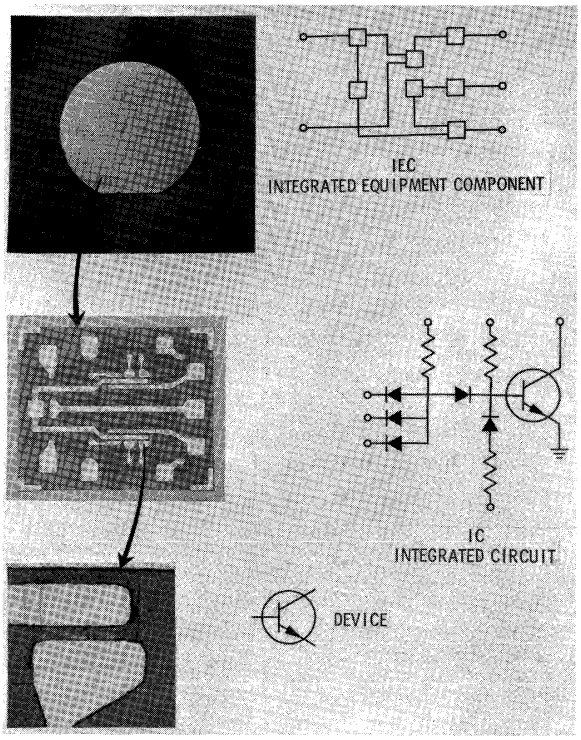


Figure 4. Pictorial view of integrated equipment component (IEC), integrated circuit (IC), and semiconductor device.

(thin film transistor) now offers a method for achieving an active element as an integral part of thin film technology; cryoelectronics, where logic, control, and memory functions are processed in compatible steps; and compound-materials technology, where more than one material may be involved in the processing.

Applicability of LSI Technology to Linear as Well as Digital Functions

It is clear that LSI technology is directly applicable to digital functions; the impact on linear functions is not so clear. A chief characteristic of digital functions is that signals are propagated through many levels of logic with no basic change in the signal level. The power gain supplied by the active element compensates for losses in the system. However, the signal level stays at the same amplitude (generally about 1 V for silicon circuits). Thus, long chains of logic functions can connect together with a high degree of repeatability of the basic logic circuit (normally a NAND or NOR gate). Consequently, digital functions lend themselves rather naturally to LSI technology.

Linear functions are generally concerned with changing the level of the signal function. For example, in a low-noise amplifier the signal level is amplified from a few microvolts to a level of a few volts. Since there is a finite lower level (set by noise) and a finite upper level (set by the particular application) over which amplification must occur, a finite number of stages is required for linear applications. An initial judgment is that array technology will not have a major impact on linear functions.

However, one must temper this conclusion because there is a large class of linear functions that requires a number of parallel channels, each identical. Consider as an example a solid-state replacement for a vidicon. With an array of photodetectors, it would be desirable to place a linear amplifier at each detection point in order to build up the signal level before it is multiplexed into a single channel. Thus, an array of photodetectors, combined with linear amplifiers, is an example of array technology impacting linear functions.[6] Arrays of compound semiconductors, consisting of photodetectors and linear amplifiers, offer a possibility of vidicon-like sensors operating in the infrared spectrum. There are other examples, including sense amplifiers for memories and light displays.

General Aspects of Large-Scale Integration Technology in Semiconductors

The calculations of Fig. 1 suggest that silicon slice processing has the potential of fabricating complete equipment components (IEC's) on a slice of silicon. Let us now outline the basic technological approaches being pursued for accomplishing this end. With the semiconductor approach, two broad areas of effort can be identified as discussed below and shown in Fig. 5 and 6.

Device-Based Design. The left side of Fig. 5 shows the approach which seeks to achieve complete equipment components by incorporating a relatively large number of devices within an area of silicon. This type of IEC is designed directly from devices and no particular effort is made to define unit circuits. The important distinction between this approach and the multifunction integrated circuit is that IEC's are achieved by incorporating many more interconnections on the chip. A typical example of an IEC made by this approach is a 50-bit MOS shift register.

Circuit-Based Design. The second broad approach to large-scale integrated electronics is shown schemati-

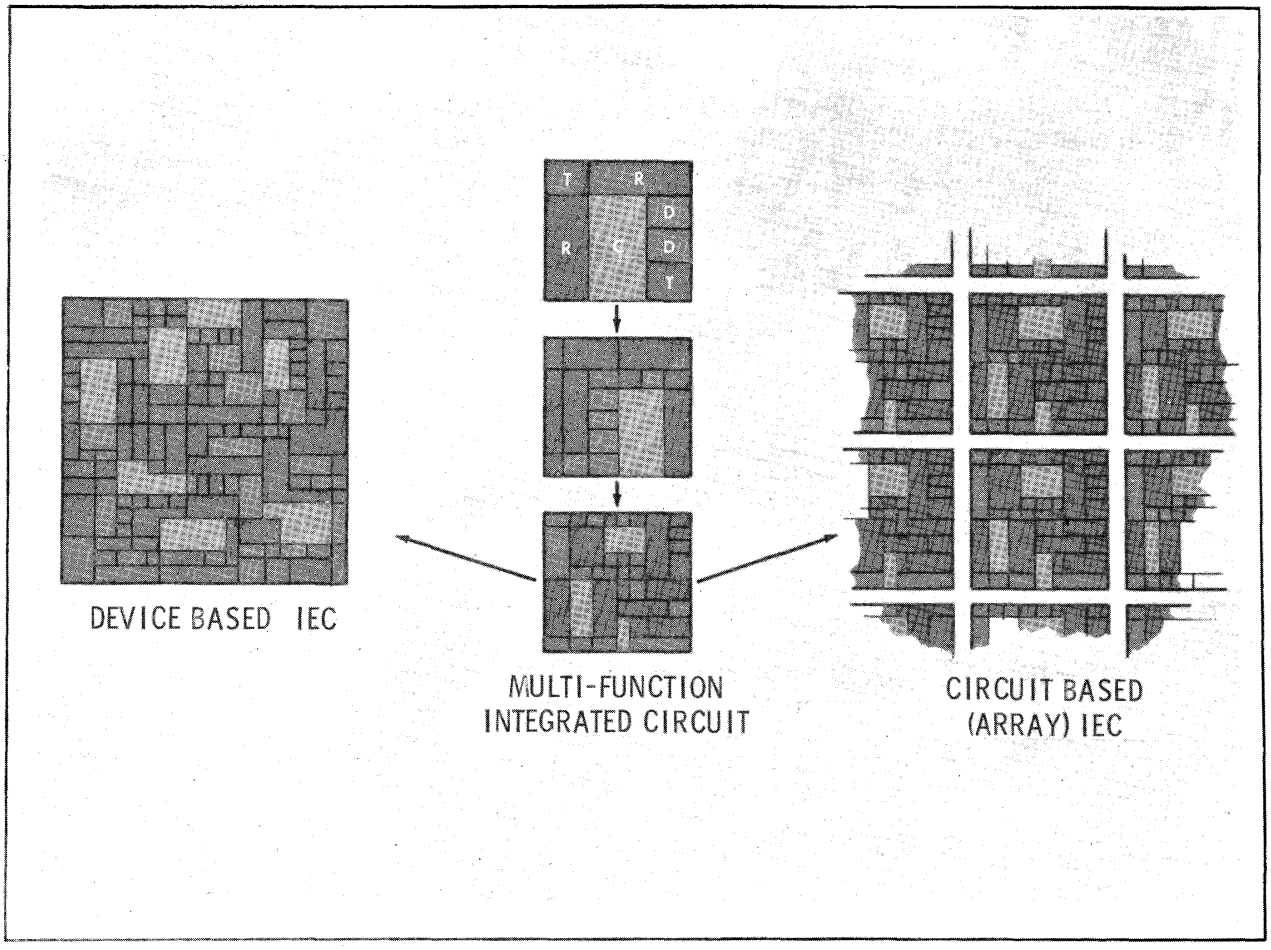


Figure 5. Evolution of integrated electronics.

cally on the right side of Fig. 5. Here, unit cells consisting of circuit functions such as NAND gates or flip-flops are the basic building blocks. This type of IEC is formed by interconnecting an array of unit circuit cells. We will use the term array for this approach.

The unit cell may be a simple NAND-NOR gate, occupying, for example, an area 10 by 10 mils. More than a single unit cell may be used and they may be intermixed. The step-and-repeat optical process allows for repetition and intermixing of the unit cells over the entire slice of silicon.

The distinctions between the device-based and circuit-based (or array) approach to large-scale integrated electronics will be developed in more detail in a later section of this paper ("Discussion of Selected Aspects"). Before doing this, we will discuss basic devices for use in large-scale integrated electronics.

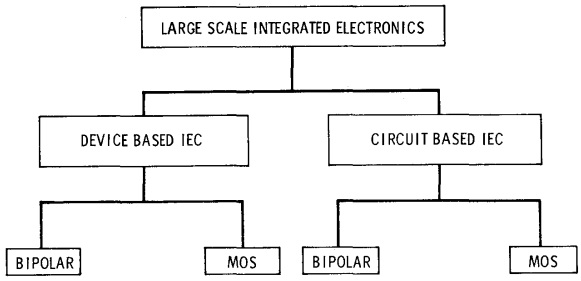


Figure 6. Large-scale integrated electronics.

BASIC DEVICES FOR USE IN LARGE-SCALE INTEGRATED ELECTRONICS

Two active device structures that will be considered for LSI application are the bipolar transistor and the MOS transistor.

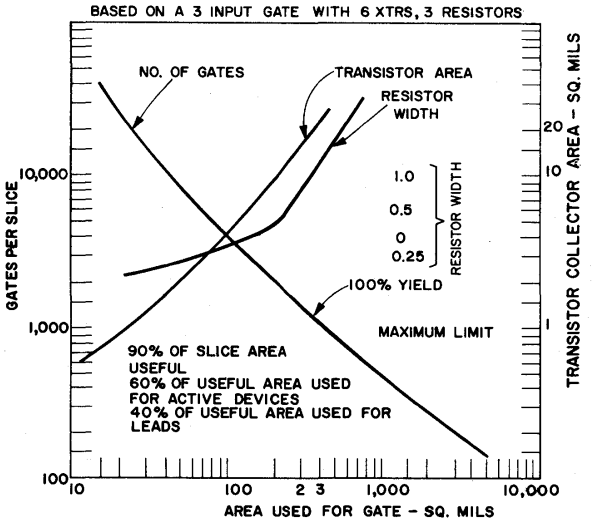


Figure 7. Bipolar transistor and gate densities for 1-inch slice diameter.

Bipolar Transistor

The bipolar transistor has made the transition from a two-sided device to a one-sided device suitable for integrated circuits in an effective way. Numerous techniques have evolved, from triple diffusion to dielectric isolation, for processing one-sided transistors of high performance. The area requirements for transistors have decreased consistently over the past five years. Fig. 7. shows that 10,000 to 50,000 gates can be fabricated in a 1-inch slice of silicon by providing transistors of smaller collector area along with smaller resistors. Thus, bipolar transistors can provide for the high density packing required for large arrays.

MOS Transistor

The MOS transistor is outlined in Fig. 8 and some of its key properties are summarized in Fig. 9. It is inherently a single-sided device, self-isolating, and occupies a small area. The MOS device can be connected to form a load resistor as shown in Fig. 10, and in Fig. 11 the area is plotted that is required to achieve values of resistance by MOS, diffused and thin film technology. Figure 11 shows that the MOS device is a convenient way to achieve impedance levels of 100 kΩ in a small area. The ability to fabricate low-power, medium-speed circuits in a small area using MOS active devices and MOS load

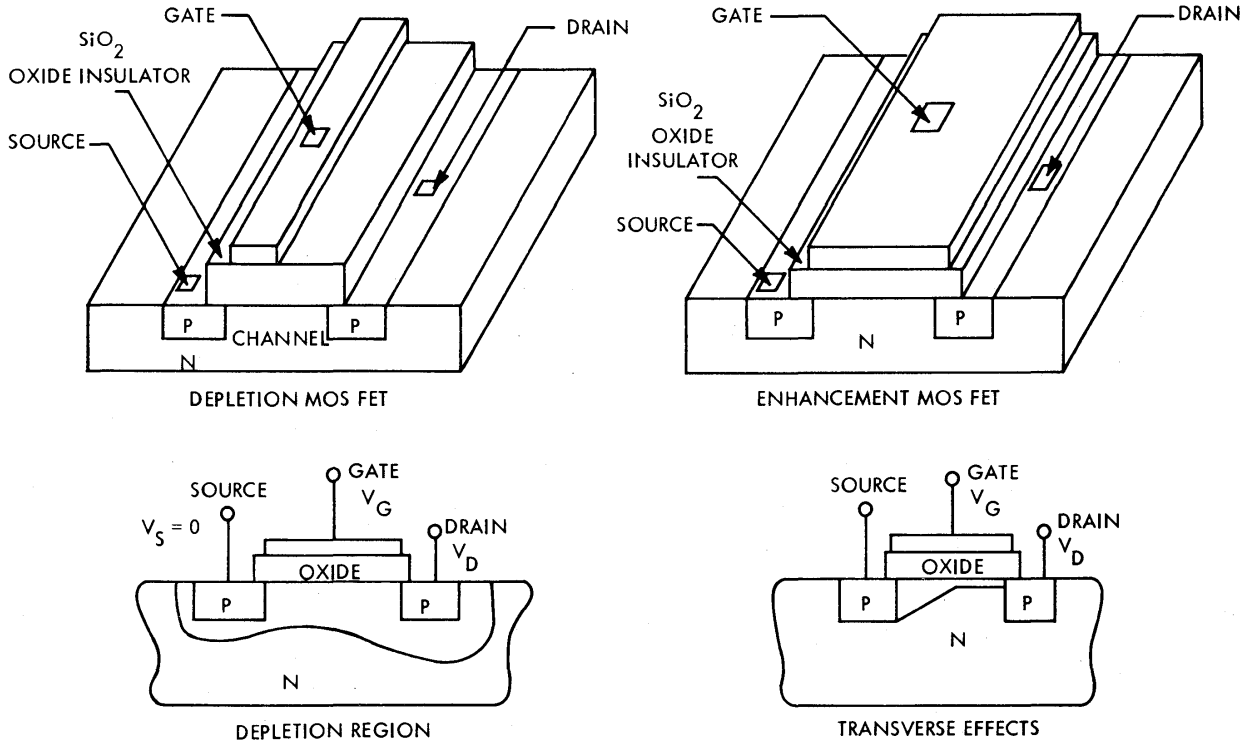


Figure 8. MOS enhancement and depletion models.

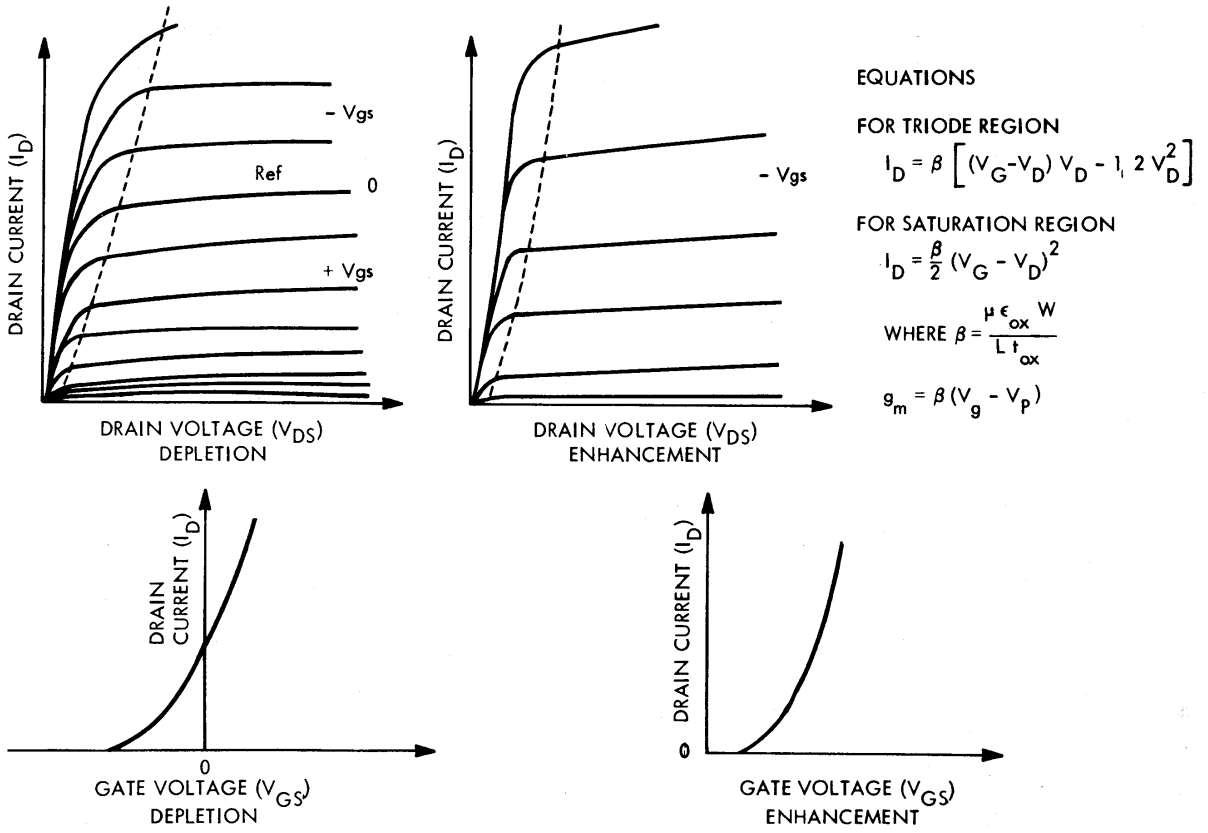


Figure 9. Characteristic curves for MOS transistor.

resistors is an attractive application of MOS technology.

Another promising application of MOS technology is in the use of N-channel and P-channel MOS devices in complementary circuits as shown in Fig. 12. This configuration will provide switching speeds in the 25–50 nsec region, with extremely low DC power drain (0.01 μW). However, it does not have the processing simplicity of the single-polarity MOS structures.

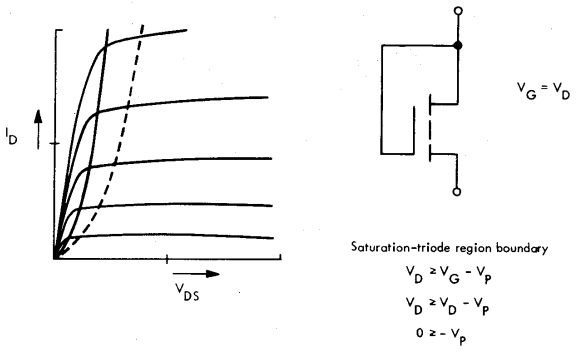


Figure 10. MOS connected as a load resistor.

Applicability of Bipolar and MOS Transistor for LSIE

With these general characteristics of both MOS and bipolar at hand, let us now attempt to assess the merits of each for specific LSI applications. A first consideration is the device densities that can be achieved, leaving aside for the moment the question of yield. Figures 13, 14 and 15 show the areas required in terms of a fundamental width W for the bipolar device with load resistor, the MOS device (assuming it also is used as the load), and the basic inverters using the two devices. From these considerations device densities are forecast as shown in Fig. 16. This figure shows that single-polarity MOS is capable of higher device densities than bipolar by at least a factor of two. A principal reason for this is that no isolation diffusion is needed for MOS; it is inherently self-isolating. The figure also shows that today we are working with MOS device densities of 100,000/in^2 and bipolars of 50,000/in.^{2} The figure also forecasts a density limit of about 10^6 devices/in^2 because of interconnection area requirements.

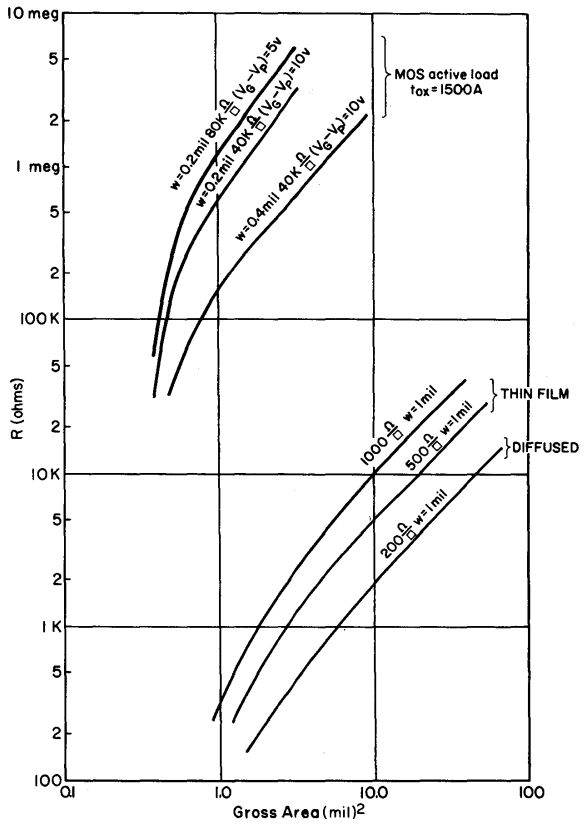


Figure 11. Load resistance vs slice area for MOS active load, thin film, and diffused resistors.

The lower density of the discretionary curve is because of the area used by redundant devices.

A second consideration between MOS and bipolar is the speed-power relationship per unit of silicon surface area. Analysis [7] results in Fig. 17, which shows a clear superiority in bipolar where speed

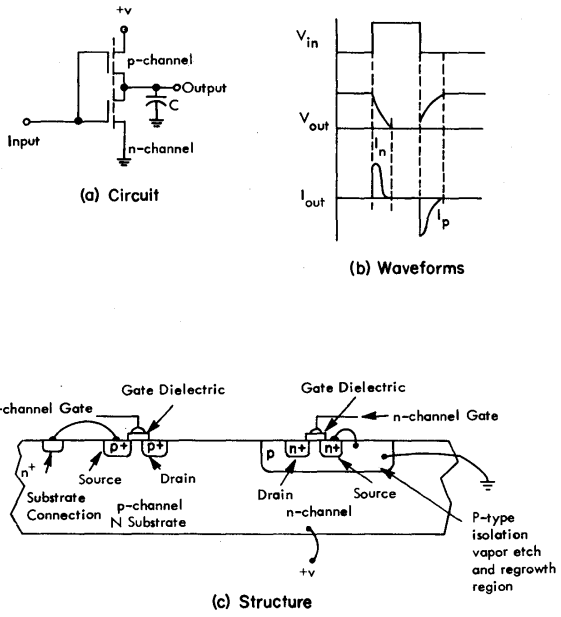


Figure 12. Complementary MOS structures and circuits.

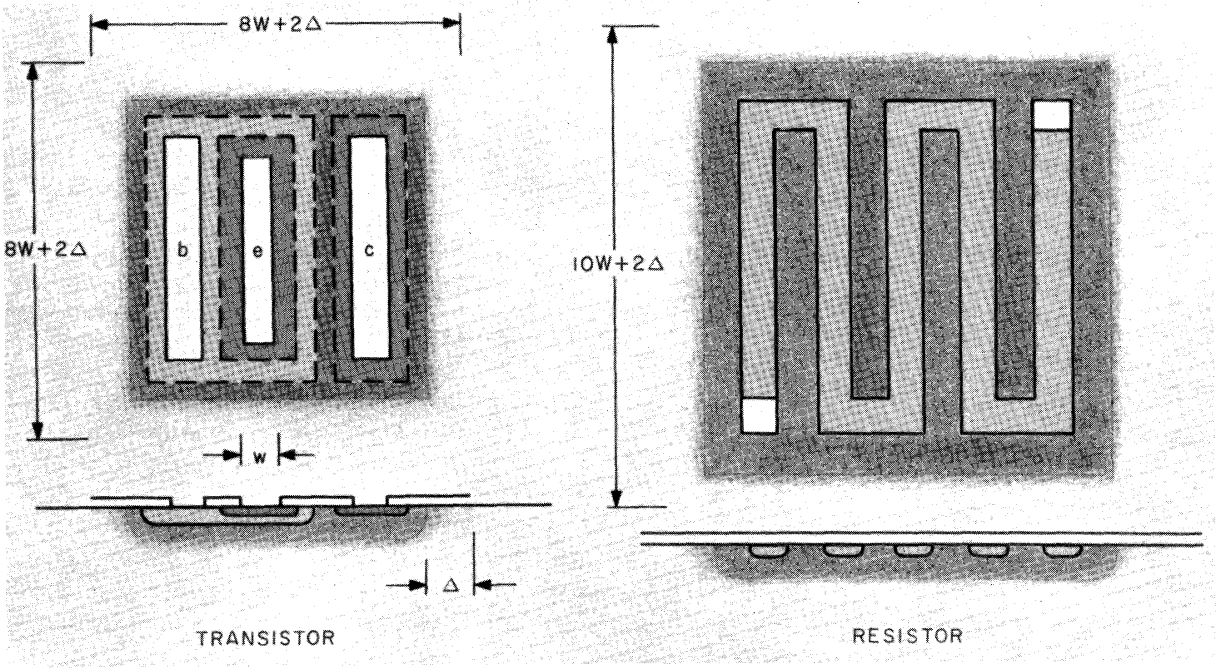


Figure 13. Area for bipolar transistor and load resistor as function of resolution width W.

and/or power is required. This superiority relates to the inherently higher gain (transconductance) of bipolar over MOS. The importance of g_m is that it is a measure of a devices' ability to charge capacities, which in turn is a measure of a device's switching speed. Figure 17 shows that at 1μA, for the same area A and capacity C, the g_m of a bipolar transistor is 40 μmhos, while that of an MOS transistor is 4.5 μmhos. To achieve a g_m of 40 for the MOS requires an area and capacity increase of 100 times. At higher currents the superiority of the bipolar over the MOS transistor is even greater.

From the two comparisons developed above, device densities and speed-power relations, we can reach some general conclusions as to the applicability of MOS and bipolar technologies. For those applications where MOS has sufficient speed and current handling capability, it should win out on the basis of achieving higher complexity per unit of chip area. Examples today include shift registers in the megacycle speed range where the capacity loading of devices is small because the fan-out is basically one. Some remarkable achievements have already been made in employing serial logic using MOS for small processors such as desk calculators.

On the other hand, bipolar will be the choice for parallel logic organization, particularly if speed is a factor. The basic advantage of the bipolar is its inherently high transconductance (g_m); therefore, it is superior where appreciable capacitance must be charged as in parallel logic.

We forecast a large applications area for both technologies, and as our technological capability increases to where both kinds of devices are processed together on the same slice in monolithic structures, another very large area of application. Finally, while our discussion has been limited to bipolar and MOS device structures, many other device types, e.g., Schottky-barriers, will be integrated into LSI structures.

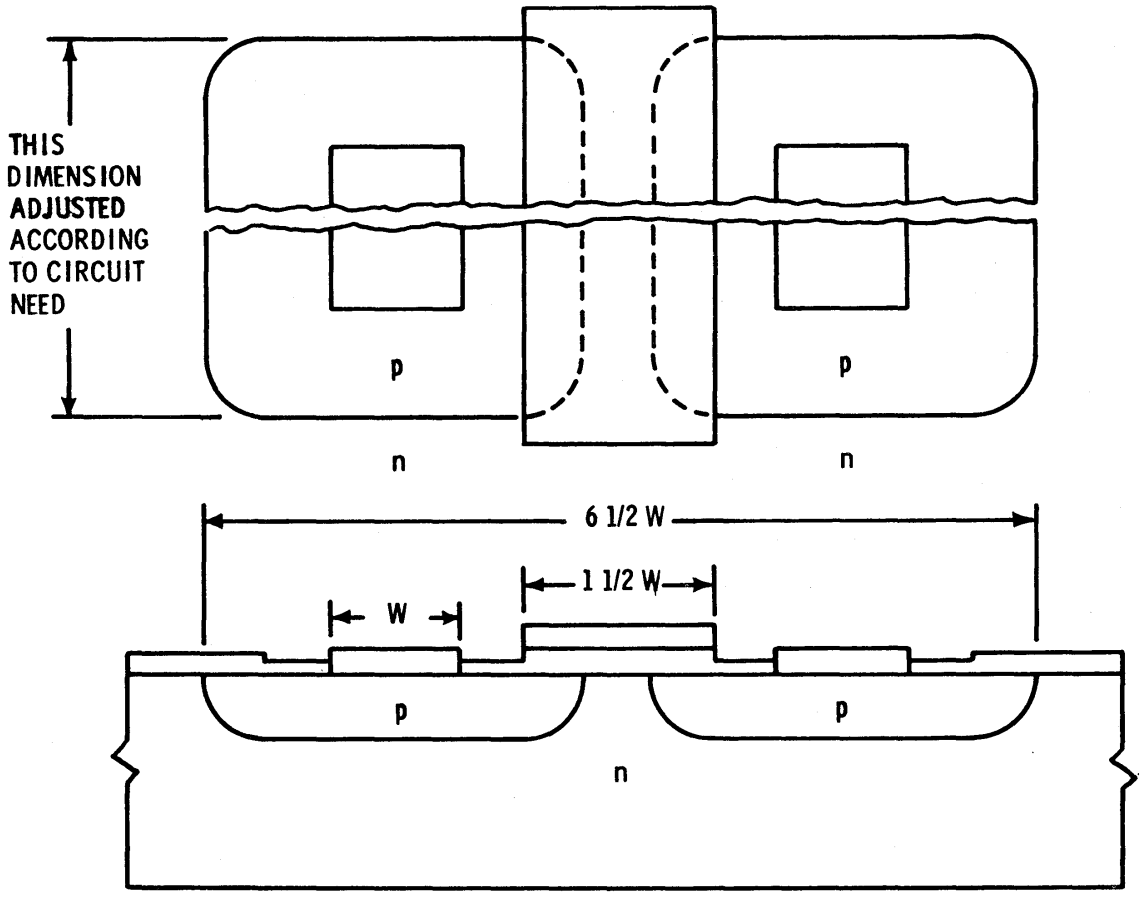


Figure 14. Area for MOS transistor and MOS resistor as function of resolution width W.

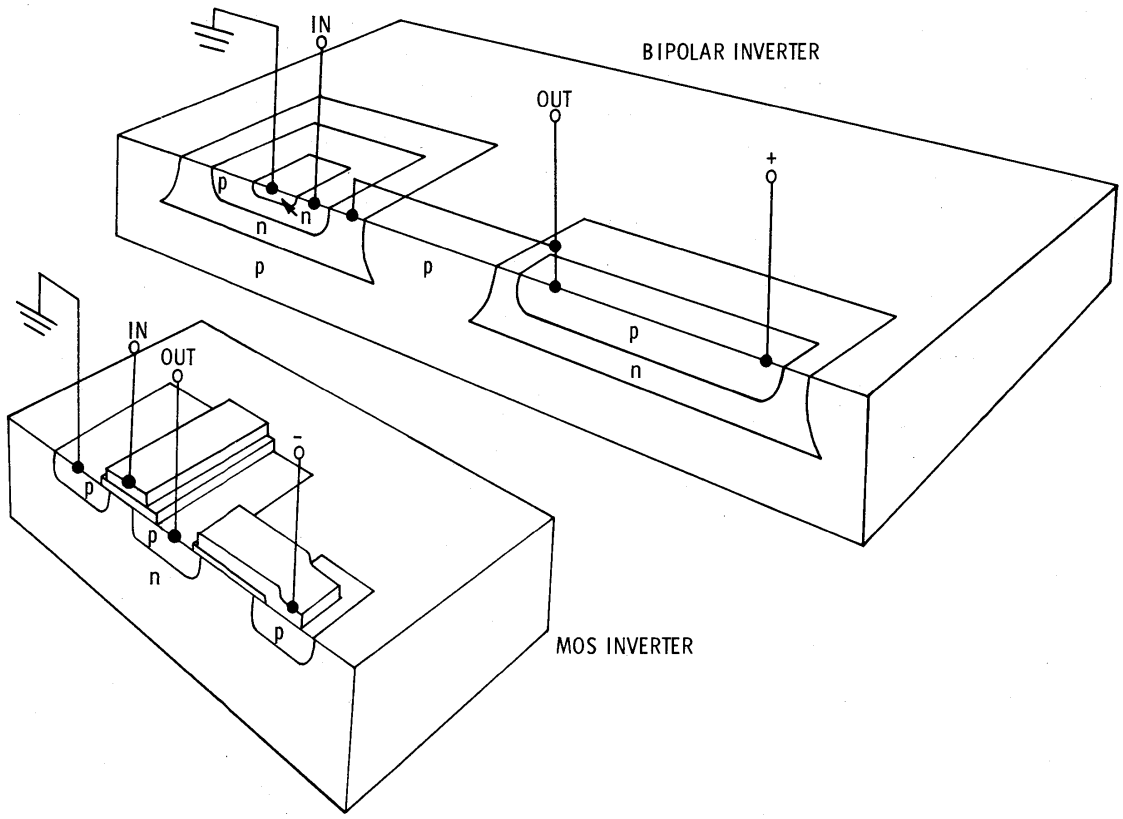


Figure 15. Basic inverters for MOS and bipolar.

DISCUSSION OF SELECTED ASPECTS OF LARGE-SCALE INTEGRATED ELECTRONICS

We now discuss key aspects of LSI, including more detail on the device-based and circuit-based approaches, discretionary wiring, forecast of level of integration to be achieved over the next 10 years, design by computer, standard products versus flexibility to custom requirements, and special requirements for subnanosecond arrays.

Device-Based Approach to LSI

The device-based approach is the natural extension of multifunction integrated circuit design and differs from the latter in that equipment components are designed and processed rather than circuit functions. Consider for example the design and processing of a 50-bit MOS shift register. The design is worked out using MOS active devices and MOS load resistors in an optimum fashion, without any attempt to partition the shift register into circuit building blocks.

The chief advantage to this approach is that one can achieve a very high density of devices, or conversely, achieve an IEC in a small area. Table 1 and Figures 18a and 18b show typical IEC's made from bipolar and MOS devices: MOS achieves higher device density, but at lower speed as discussed above.

The entire IEC, or at least a major part of it, is achieved within a relatively small chip size. A characteristic of this approach is that 100% yield is required over the chip area (e.g., 100 × 100 mil), but not over the entire slice. Consider for example a 1.50-inch diameter slice where

$$\text{Number of chips} = \frac{\text{slice area}}{\text{area/chip}} = \frac{\pi\ 9/16}{100 \times 100 \times 10^{-6}} = 175$$

If 50 of these 175 chips are good, the overall material yield is 35%.

While discretionary wiring techniques are not used within the chip areas (100% yield is demanded here) it is possible that discretionary wiring will be used

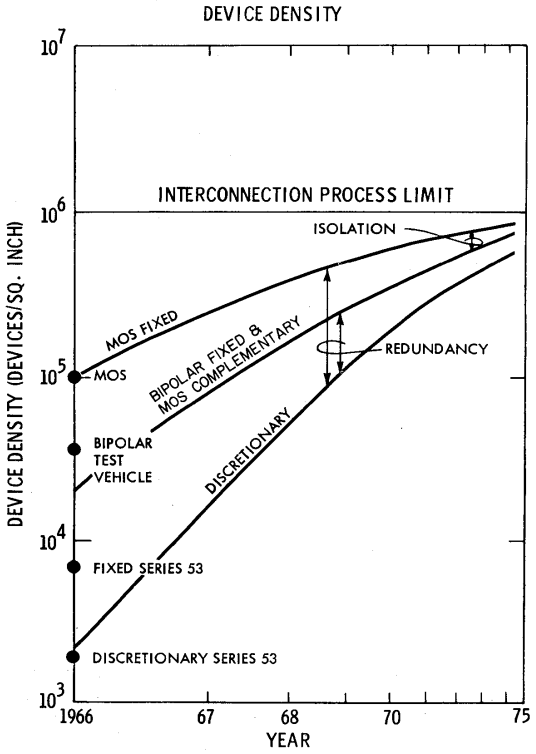


Figure 16. Ten-year forecast of device density.

to wire together N good chips in a slice to form a more powerful function. In the example above, the 50 good chips might be connected together without scribing the slice into individual chips. One reason for doing this is that the oxidized silicon surface provides an excellent surface on which metallic transmission lines can be deposited.

What are the chief handicaps or limitations of the device-based design approach to LSI? Probably the most important limitations are its lack of adaptation to change and long-time cycle for implementation. Each IEC design requires a complete set of masks, including diffusion and metallization. While some flexibility can be attained at the metallization level by providing extra devices in the chip (master slice concept), the approach is most suitable for standard products where relatively large production runs occur, or for custom designs of high volume.

In summary, the device-based approach to large-scale integrated electronics is already off to a fast start. For the case of bipolar technology, the IEC's are being designed to give added logical power and capability to existing IC product lines, as for example, three of the TI units listed in Table 1 augment the Series 54 line. For the case of MOS, the leading edge of this technology has aimed towards serial logic systems designed around shift registers.

Array or Circuit-Based Approach to LSI

In this approach circuits are used as the basic building blocks for designing and processing the IEC's. A number of advantages occur when one moves the building block level from the device to the circuit function. A key advantage is that Boolean logic equations are readily expressible in terms of NAND, NOR and related logical decision circuits. These equations, which are basic to the design of computers, are independent of the devices underlying the Boolean circuit element.

Another advantage is that it is possible to incorporate a high degree of flexibility into the process technology. Consider the problem of an IEC manufacturer responding to a customer's request for a specific IEC. Assume that the customer presents the IEC manufacturer with Boolean equations and specifications. Let us examine the different methods (see Table 2) by which the manufacturer may respond. We will assume that silicon slices are

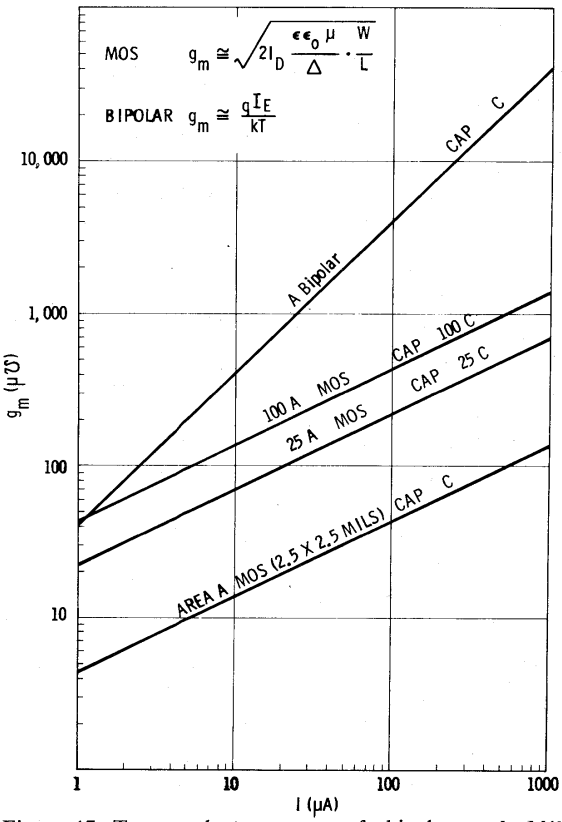


Figure 17. Transconductance g_m of bipolar and MOS transistors vs current and device area.

Table 1. Integrated Equipment Components–1966

Mfr.	Component	Device	Area *in* ^{2}	No. of Devices	Device Dens. *devices/in* ^{2}	Speed *nsec*	Power *mW*	Pads
TI	Series 53 Array	Bipolar	0.7	1,200	1,720	35	1200	60
TI	8-Bit Shift Reg	Bipolar	0.006	160	26,500	15 mHz	190	6
TI	Honeywell Memory	Bipolar	0.0071	100	14,000	25	250	14
TI	Parallel Load Serial Shift	Bipolar	0.01	150	15,000	25	270	22
GME	A-C 100-Bit Shift Reg	MOS	0.0065	613	94,500	1 mHz	200	12
GI	D-C 21-Bit Shift Reg	MOS	0.0042	158	37,600	500 kHz	150	11
TI	22-Bit Shift Reg	Bipolar	0.0126	350	27,800	3 mHz	35	8
TI	B to D Decoder	MOS	0.0057	152	26,700	200 kHz	25	26

processed with 100% yield of unit cells—the question of dealing with cells on the slice that are not good will be discussed below, under "Discretionary Wiring."

For those requirements where the logical function (IEC) can be built by connecting together identical unit cells (e.g. NAND gates), the manufacturer need only make masks which provide for interconnecting gates in a specific pattern. Processed slices would be on hand which have a large number of NAND gates. Such slices would have a first level of metallization on them as indicated in Category I, Table 2. Only new masks for 2nd and 3rd level metallization are required to meet a customer's specific request. More flexibility can be incorporated into this approach by providing more than one kind of unit cell on the slice. For example, a slice with a mixture of gates and flip-flops will meet a large proportion of computer requirements. This approach provides very fast response to customer's needs.

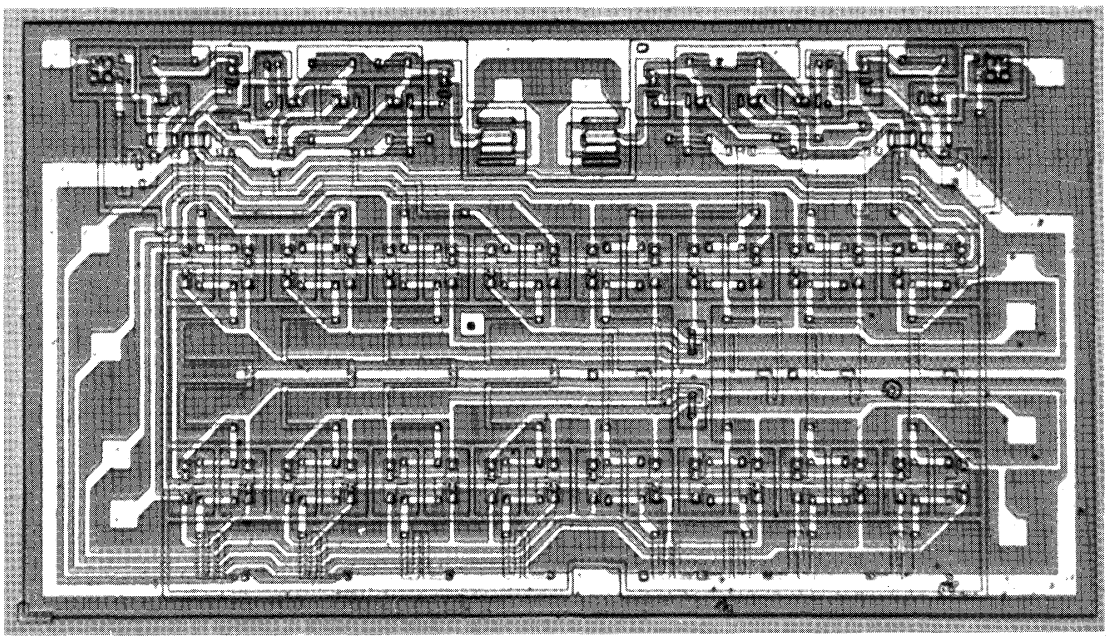
A second approach, Category II, involves processing slices which have a common master unit cell through the diffusion and third oxide removal operations. This master unit cell would have sufficient devices such that 10 to 15 different logical circuits could be attained by variations of the first level of metallization. Coupling this with the ability to interconnect the unit cells together in specific ways provides a high degree of flexibility. However, this requires a first-level metallization mask as well as a second (third if necessary) level mask.

The third approach is to generate a complete set of masks for each order, as in Category III, Table 2. A complete set of diffusion masks are required, along with first level metallization masks (second and third if necessary). This is the most expensive approach

Table 2. Categories of Array Approach to LSI

Process	Definition Category I	Definition Category II	Definition Category III
Oxidation	1st Oxide Removal (OR)	1st OR	1st OR
Collector Diffusion	2nd OR	2nd OR	2nd OR
Base Diffusion	3rd OR	3rd OR	3rd OR
Emitter Diffusion	4th OR	4th OR	4th OR
Metal Deposition	1st Level Leads	1st Level Leads	1st Level Leads
Insulation Deposition	2nd Level Insulation	2nd Level Insulation	
Metal Deposition	2nd Level Leads	2nd Level Leads	
Insulation Deposition	3rd Level Insulation		
Metal Deposition	3rd Level Leads		

Operations in boxes permit component variability.



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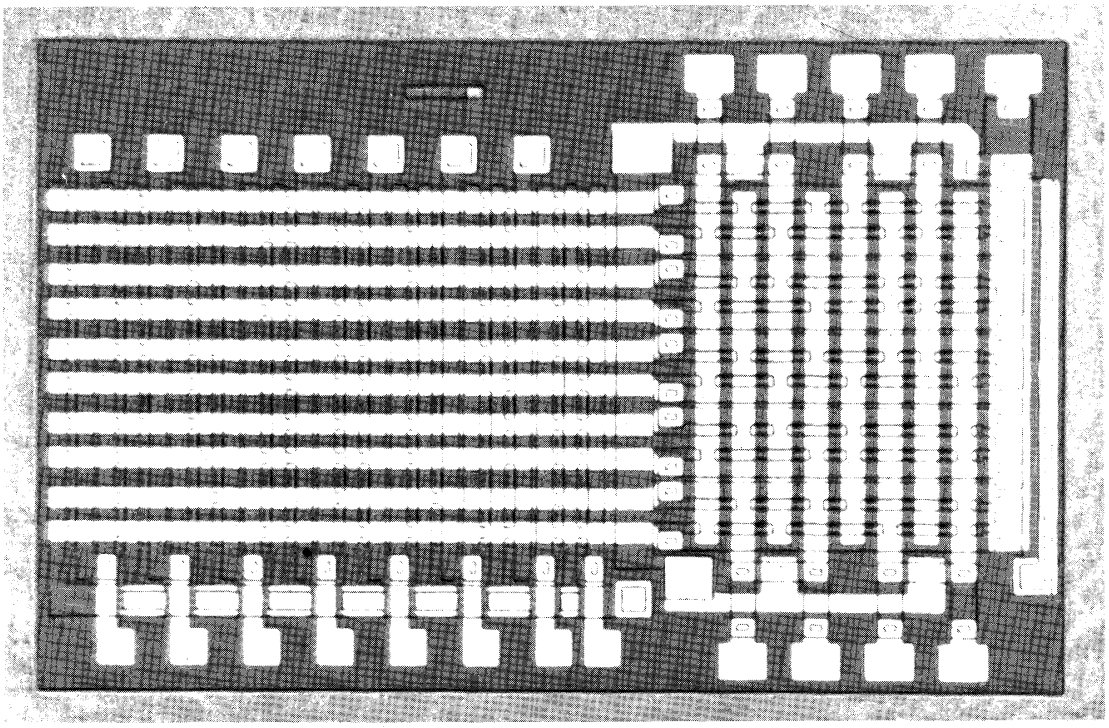

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Figure 18. Examples of device-based IEC's—characteristics in Table 1. (a) Eight-bit bipolar IEC. (b) Binary-decimal decoder MOS IEC.

from the initial design phase and the most time consuming, but it can provide savings in materials usage and therefore may be favored for longer production runs.

A comparison of the approaches of Table 2 reveals that Category I provides the fastest turn-around time and lowest initial cost but has the poorest utilization of unit cells in the slice. Category III provides the best usage of area in the slice because it has no cells or devices that are not used, but is the slowest in turn-around time and has the highest initial expense. Category II is midway between I and III in all respects.

All three categories are under development in the semiconductor industry. Prediction of the relative costs and degree of usefulness of these approaches is difficult at this time because of the embryonic state of the technology.

Discretionary Wiring

The goal of processing technology is 100% yield of unit cells over the slice. For the same reason that integrated circuit yields are much higher than were expected, considering arguments based on discrete device extrapolations, array yields will be much higher than predicted from simple extrapolations of integrated circuit yields. However, at some array size one can expect that defective unit cells will become a problem which will affect overall array yield. It is desirable then to develop a system whereby defective cells can be omitted from the interconnected array.

The problem of achieving discretionary wiring at low cost relates to testing, automatic mask making, and computer programming of interconnection systems. It should be emphasized that successful implementation of the discretionary approach demands a rapid, low-cost mask-making procedure since each slice may require a different interconnection pattern because the "good" cells will occur in different locations. Figure 19 shows an approach to discretionary wiring which is being developed at Texas Instruments Incorporated under sponsorship of the Air Force Systems Command, Wright-Patterson Air Force Base.[8] At the top left of the figure a silicon slice is shown which has an array of unit cells. The unit cells consist either entirely of NAND gates and flip-flops, or a mixture of the two. A first level of metallization is provided on these cells so that they can be probed by multiprobe test equipment. The

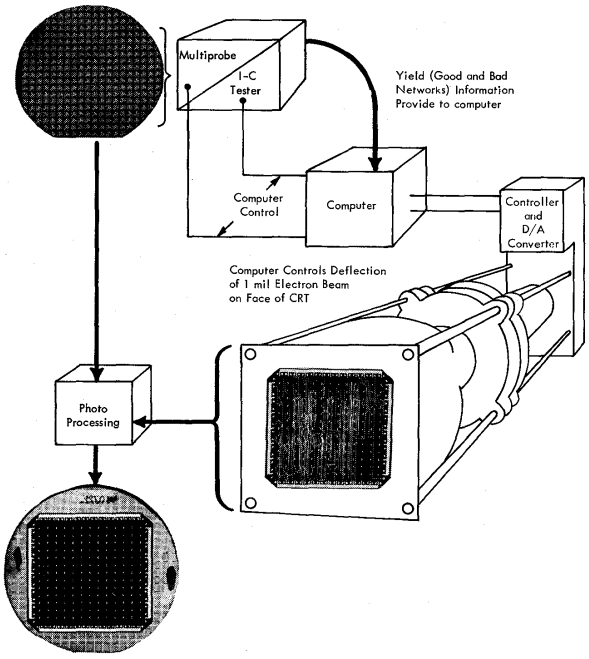
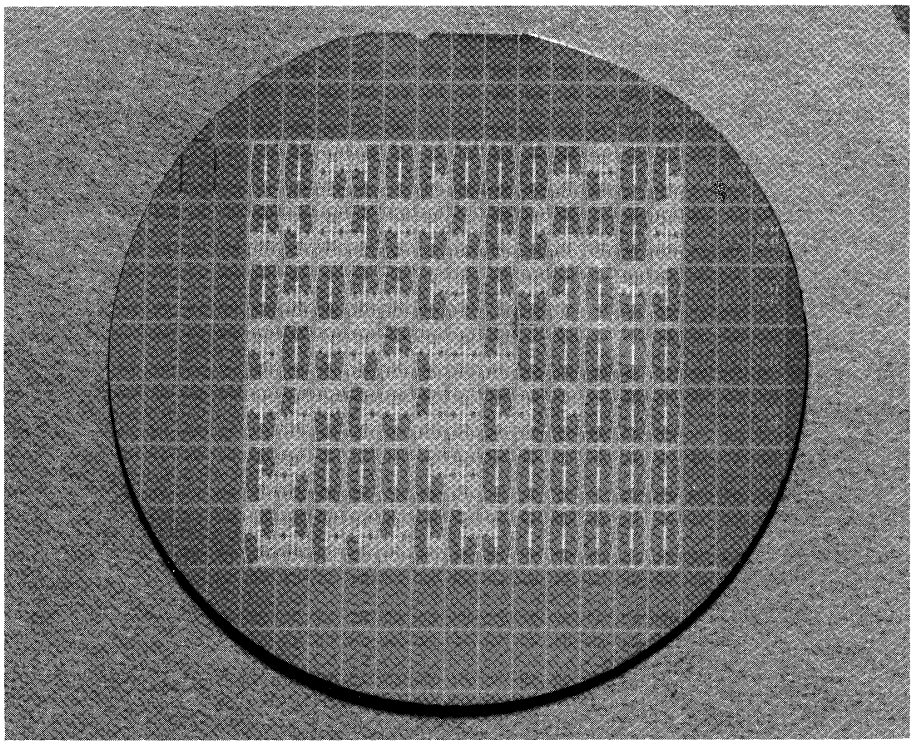


Figure 19. Discretionary wiring system being developed by Texas Instruments under Air Force sponsorship.

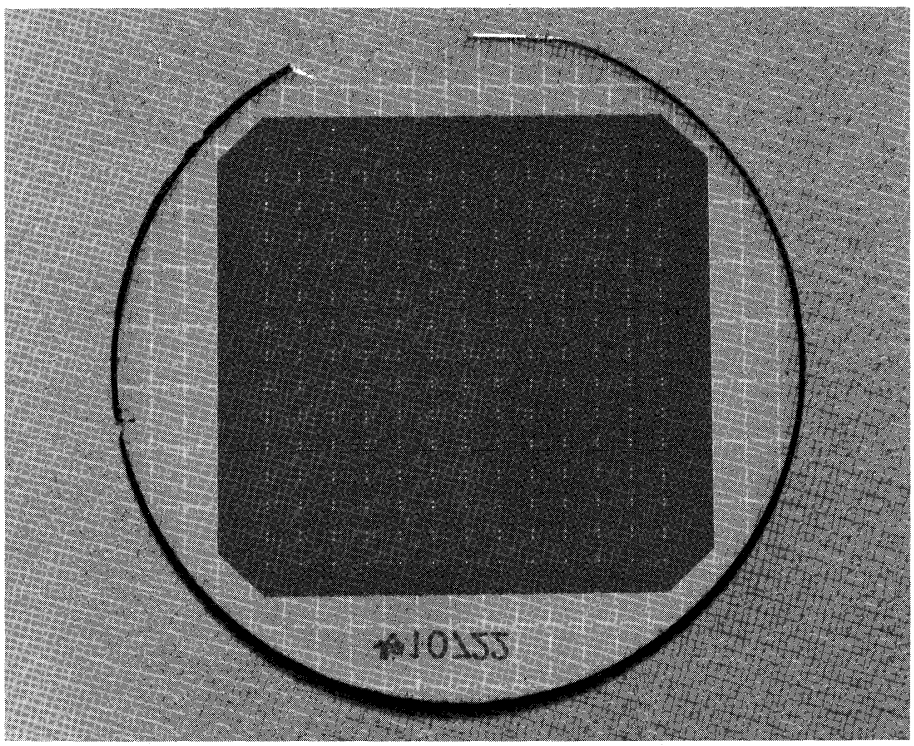
information concerning location of good and bad cells is fed into the computer, which generates an interconnection pattern. The control for each pattern is fed to the high-resolution CRT, and a pattern is generated on the face of the CRT. This pattern is projected on photosensitive material to form a photomask. Finally the set of masks is used to process interconnection patterns on the semiconductor slice.

All elements of this system are under active development. It is planned to have the system in operation during the last half of 1966.

To illustrate the discretionary wiring approach the series of pictures in Fig. 20 are given. Figure 20a shows a slice where the "good" gates to be used in the array have the first level of metallization applied. Each rectangular area contains four Series 53 gates, and the full array consists of 120 "good" gates. The slice with a layer of insulation applied and holes etched through to the first level metal are shown in Fig. 20b. Horizontal interconnections which were designed by the computer are shown in Fig. 20c. Figure 20d shows another level of insulation applied and holes etched through to the second level of metal. Figure 20e shows the third and final level of metallization which completes the interconnection of the 120 gates.

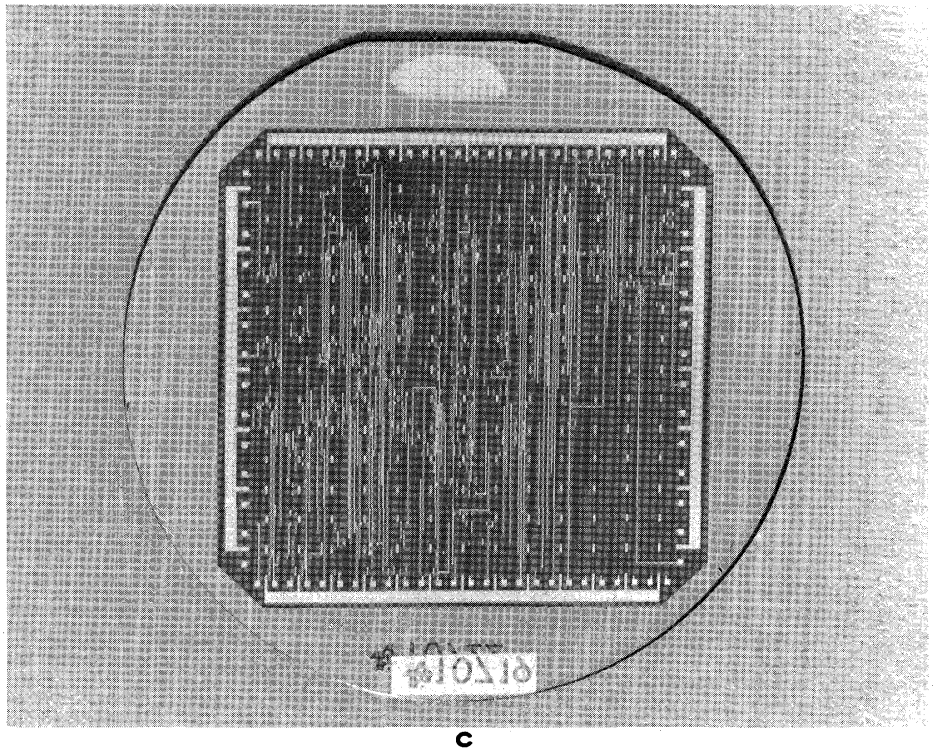


a

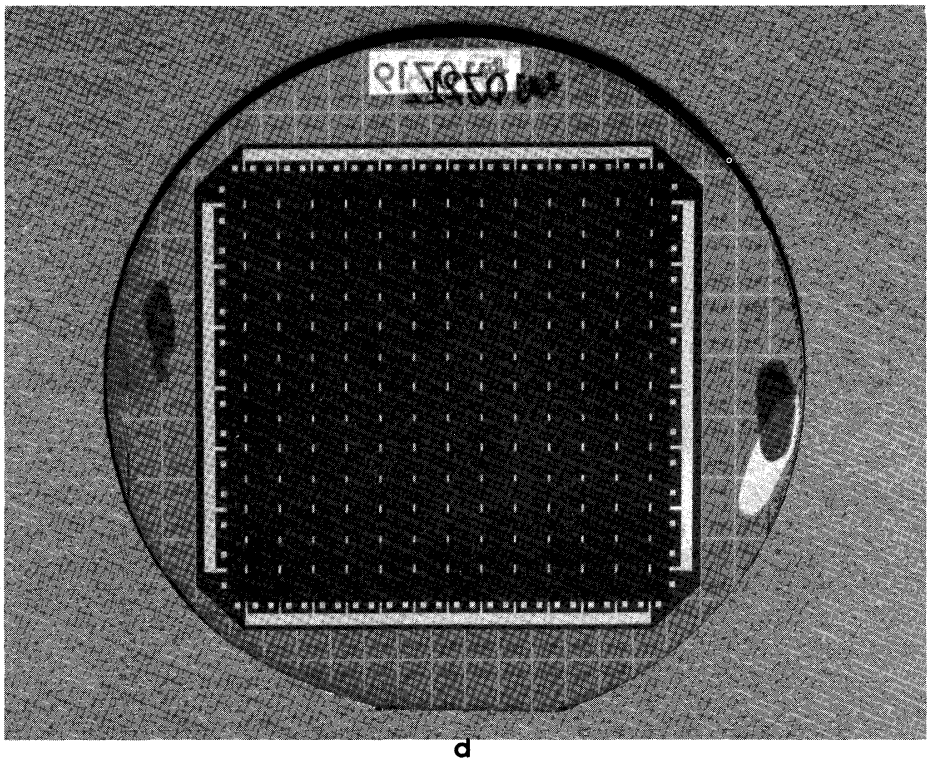


b

Figure 20. Series 53 array of 120 gates (process description in text).

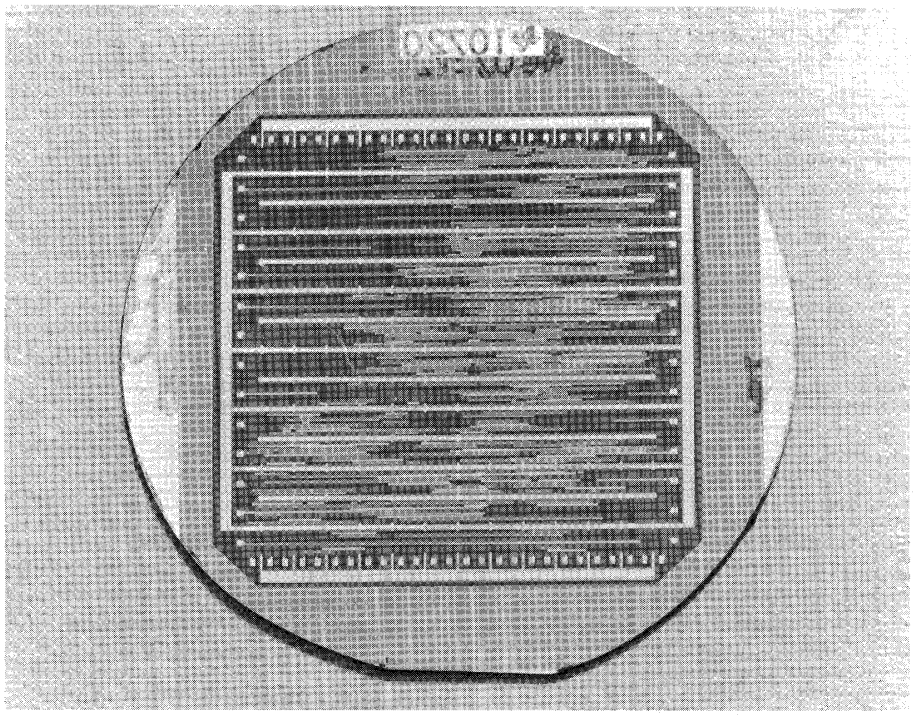


c



d

Figure 20. *continued*



e

Figure 20. *continued*

While the masks for the above example were cut by normal techniques, the system shown in Fig. 19 will make this an on-line process of short-time response. Characteristics of this array (the Series 53 array) are shown in Table 1. Comparison shows that this array has nearly 10 times the number of bipolar devices than the other bipolar IEC's, which are of the 100% yield category.

An important aspect of the discretionary approach is that it will allow for integrating to higher levels of complexity at any given time than will the 100% yield approach. For example, the aforementioned program has a minimum goal of 250 gates per slice or 2500 devices per slice, and a maximum goal of 1000 gates per slice or 10,000 devices per slice; furthermore, the arrays will be ready for production by the end of 1967. It is believed that this is an order of magnitude higher performance than will be achieved by 100% yield methods in the same time period.

We note that this approach to discretionary wiring has much in common with the process of Category I in Table 2. The interconnection pattern generator can be used to generate the second and third level masks required in Category I. If one has 100% yield over the area of the slice to be used, the probing step is eliminated. Also, the computer programs for pattern generation will be somewhat simpler because the location of gates is known.

Forecast of Degree of Integration of IEC's

Our forecast of device density in Fig. 16 over the next 10 years was relatively simple to make since it was derived from reasonably well-defined parameters. In contrast, the forecasting of the level of integration of IEC's over the next 10 years is a much more complicated and less precise task. Subjective as well as objective points must be considered. However, it seems worthwhile to discuss some of the aspects of the problem and to arrive at a "forecast," even though admittedly it is unprecise.

Let us first define what we mean by level of integration. By this we mean the total number of good devices that will be interconnected on a single monolithic chip of semiconductor material (presumably silicon). We will not discuss the "chipping within a package" approach.

A first consideration is the theoretical device density, shown in Fig. 16. The MOS and Bipolar

Fixed curves imply 100% yield or fixed interconnection pattern (FIP). The Discretionary curve indicates a lower density because of the area required for redundant devices.

A next consideration is the chip size itself. Here we must consider a number of factors including single field of view optical limitations, step-and-repeat optical techniques, crystal size, and process yield limitations.

Optical problems limit the area over which high resolution can be achieved in a single field of view. Figure 21 shows the capability of the best of today's lenses, and the 10-year forecast. A 100 × 100 mil area with 0.2 mil lines is representative of today's integrated circuits production. The area will increase to 300 × 300 mil and resolution should approach the wavelength of light. New techniques such as electron beam will be required to achieve further improvements, but we will not consider these possibilities in the discussion.

Step-and-repeat techniques allow for the stepping of a fixed field of view over much larger areas. This process is used in today's production technology such that 100 × 100 mil or smaller patterns are stepped over slices 1½ inches in diameter.

From these considerations Fig. 22 has been constructed. The area labeled Fixed Field Pattern forecasts that fixed pattern IEC's will increase from the present 100 × 100 mil size to 300 × 300 mil size.

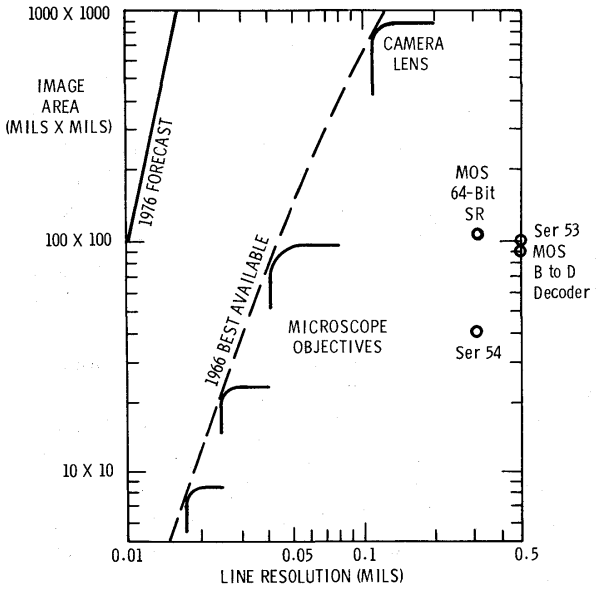


Figure 21. Optical image dimension as a function of resolution.

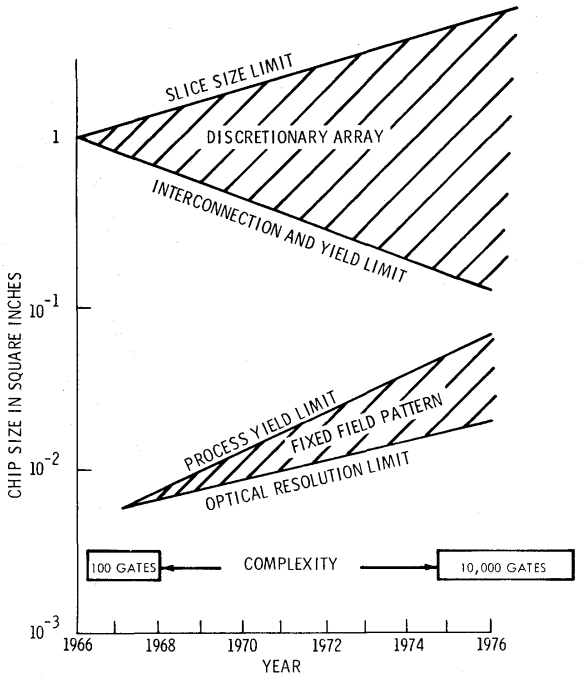


Figure 22. Chip size forecast.

The smoothness of the curves relates to the gradual increase in area over which 100% yield is achieved.

The upper shaded area is based on step-and-repeat optical techniques and discretionary wiring. The upper line shows the increase in crystal size from 1-inch diameter to 3-inch diameter material. The lower line suggests that interconnection and yield improvement will allow for smaller chips to be used because of less area required for redundancy.

Finally Fig. 23 shows the author's best judgement as to the number of devices per chip that will actually be used over the next 10 years. These curves have been developed by consideration of the factors of Figs. 16, 21, 22, and 23, by knowledge of today's capabilities (1966 data points of Fig. 23), and by the subjective consideration that 100,000 devices per chip, which will provide logic power of 10 K to 20 K gates, is a practical requirement limit. One argues that 10 K to 20 K gates provide suitable basic building blocks for computer systems.

Note that the distinction between discretionary and fixed patterns disappears in the 10-year period. It is reasonable to forecast that 100% yield will be achieved for this complexity in this period. This conclusion does not invalidate the present program on discretionary wiring. As Fig. 23 shows, discretionary wiring technology will provide for the more rapid

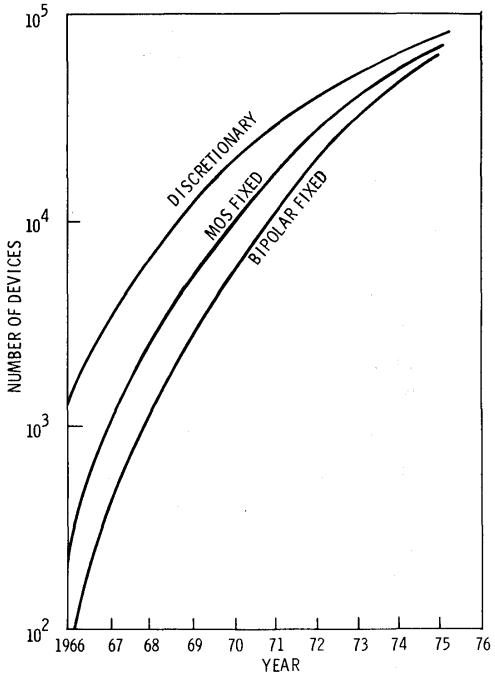


Figure 23. Forecast of number of devices per chip—IEC complexity.

development of the high-complexity IEC's that are vital for the industry.

The merging of bipolar and MOS techniques does not invalidate our previous discussion—the 100 K MOS devices will be achieved in a smaller area than that required for the bipolar devices (Fig. 22).

Our rather arbitrary limit of 100 K devices per chip does not imply a technological limit so much as a practical limit. The direction of digital system requirements, which we shall not attempt to forecast, could generate motivation to increase this limit markedly.

Design by Computer

At the levels of complexity that are forecasted for IEC's, the problem of design is a formidable one. For this and other reasons we can expect that computer-aided design will be developed. One approach is to use computer-aided design directly at the device level; that is, design IEC's by computer directly from device parameters. This is what the human does today when approaching LSI through device-based design.

However, it is likely that a more useful approach will be to use computer design at the circuit function level. Here one defines a set of logical circuits such as NAND gates, shift registers, flip-flops, etc., and utilizes a computer to design layouts which minimize crossovers, area, etc.

An important benefit of design by computer in terms of circuit building blocks is that it will shorten the reaction time of IEC manufacturers to system requirements. The systems manufacturer will state his requirements to the IEC manufacturer in terms of Boolean logic equations. The IEC manufacturer will translate these requirements to process steps in the factory using computer-aided design.

Another reason for emphasizing design by computer is that in some cases, normal breadboarding techniques will not simulate sufficiently well the actual conditions on the silicon slice. For example, MOS devices, if breadboarded as discrete devices, would be so heavily loaded down with capacity that their performance would bear little relation to that in a monolithic structure. Subnanosecond bipolar transistors, if breadboarded as discrete devices, would have such large delays between devices as compared to the monolithic case, that information gained by breadboarding would have little value.

Finally, we note that back panel "patching" techniques are not available in highly integrated structures, and so the elimination of human errors becomes especially important.

Standard Products vs Flexibility to Customer's Requirements

A key question of large-scale integrated electronics is—To what degree will standard product lines of IEC's be accepted by the equipment and systems manufacturers, or conversely, to what degree will they demand custom IEC's? Before attempting to answer this, it is perhaps worth examining what has happened in integrated circuits.

In the early days of integrated circuits considerable resistance was given to accepting the idea of standard circuits. Important custom designs have been and are continuing to be developed, and often these become the technological base for standard lines introduced at a later date. However, it is clear today that there has been far greater acceptance of standard lines by the industry as a whole than was originally predicted.

Today one hears similar arguments. For example, because integration to the equipment component level necessarily involves the computer logic, some pro-

ponents claim that IEC's will be entirely a custom business. It is the author's opinion that this will not be the case. There certainly will be considerable custom design work, particularly in the early stages of the development of the technology. However, as time goes on, the author forecasts that standard IEC's will be developed and produced that will be basic building blocks of systems. Furthermore, it is the author's forecast that we will see an even greater acceptance of standard products at the IEC level of integration than at the IC level of integration.

Special Considerations for Ultra-High Speed (Subnanosecond) Arrays

Designers of high-speed computers are faced with two fundamental problems in making computers that switch appreciably faster than about 5 nsec. The first problem is that of the transmission time between discrete components. Remembering that electromagnetic signals travel 6 inches in one nsec, one recognizes that packing densities achievable by discrete devices run into phasing problems at about 5 nsec. Multifunction circuits provide some gain here because of the increased packing density. However, the improvement gained is marginal because each gate must be capable of communication with any other gate, at least on a single multilayered board.

The second computer design problem is also very fundamental: terminated transmission line structures of low impedance ($\cong$ 50 Ω) are needed in order to interconnect gates operating in the few nsec range. This configuration is required to prevent false reflections. Devices of substantial current handling capability are thus required which, in turn, limits the density to which circuits can be packaged together.

Array technology provides solutions to both problems. By interconnecting on the slice, several hundred gates can be located within one inch of each other. Thus, phasing problems will not be encountered on the slice, at least for speeds in the range down to 0.1 nsec. For devices 10 mils apart, the transmission time will only be of the order of picoseconds.

The second point is that the proximity of gates to one another (tens of mils) makes it unnecessary to provide low transmission line impedances between gates. Instead, the interconnections on the slice can be viewed as simple capacitors, ranging in the 1/10 pF and less range. Thus, current drive capability for the active devices is reduced. This in turn allows for the appreciably higher packing densities required to minimize transmission delays.

This subject is further developed in Ref. 4. The conclusion is that LSI technology will make it possible to build computers which operate at decision switching speeds well below one nsec.

IMPACT OF LARGE-SCALE INTEGRATED ELECTRONICS

This technology promises major impact in many areas of electronics. A few of these are:

1. Lower cost data processing systems.
2. Higher reliability processing systems.
3. More powerful processing systems.
4. Incorporation of software into hardware, with subsequent simplification of software.

Pervasiveness of Electronics

A more general, very important result has been discussed by Patrick E. Haggerty in his keynote article [9] in the Special Issue of the *Proceedings of the IEEE* on Integrated Electronics. Mr. Haggerty emphasizes that Integrated Electronics will result in electronics pervading our entire social structure. Quoting from Mr. Haggerty's article:

> To say with Dr. Noble that electronics is a generic art, or for this author that electronics is *inherently pervasive,* is simply to say that the basic knowledge and the tools of electronics are so pertinent to the needs of our kind of society that the products and services which are the result of the knowledge and tools have nearly unlimited usefulness and can contribute in a major way across our entire social structure.
>
> Yet, in spite of the pertinence of the knowledge and tools, there have been very fundamental limitations to our applying this knowledge and these tools as broadly as they justify and *realizing the inherent power and full pervasiveness of electronics.* Some of the most harassing have been:
>
> 1) The limitation of reliability
> 2) The limitation of cost
> 3) The limitation of complexity
> 4) The limitation imposed by the specialized character of and relative sophistication of the science, engineering and art of electronics.
>
> The limitations are, of course, interrelated. Cost is obviously affected by the need for high reliability and necessarily complex solutions. Conversely, the

more complex the solution required, the greater the likelihood that reliability and/or cost will become a controlling limitation. Such solid-state devices as transistors and diodes have certainly led the way to marked improvement in reliability, but they have hardly eliminated complexity. The solutions we have achieved still have a relatively high enough cost to inhibit the application of electronics in those broad areas which we customarily describe as the industrial and consumer sectors of our economy. So far as the fourth limitation is concerned, electronics is indeed a sophisticated branch of engineering and as such it has required highly skilled practitioners. Yet the very sophistication called for inevitably limits the rate at which electronics can pervade our society. For electronics to be truly pervasive, it must be readily and commonly used by the mechanical engineer, the chemical engineer, the civil engineer, the physicist, the medical doctor, the dentist, the banker, the retail merchant, and by the average citizen in broader ways than just for bringing entertainment to his home. Electronics cannot be truly pervasive unless such persons whose needs call for the powerful tools of electronics are capable of using them. It hardly seems feasible to suggest that all these highly skilled practitioners in other professions must also become skilled in the internal complexities of ours. *The problem is considerably simplified, however, if the electronics skills which they require are limited to the comprehension and specification of the input and output parameters of the electronic functions they need.* And, it is exactly here that integrated electronics may prove to remove a large percentage of these communication limitations. The contributions integrated electronics is likely to make in removing limitations in the categories of reliability, cost, and complexity are also impressive. Indeed, because integrated electronics seems to have a high probability of removing an appreciable percentage of the limitations in all four categories, I believe it may bring the total of these limitations to a critical level. Subsequently, it may initiate the terminal phase in which electronics contributes in truly vital ways to all segments of our society.

Expanding upon the fourth limitation, large-scale integrated electronics, does indeed offer the promise of placing most of the problems associated with the specialized character of electronics in the hands of the materials technologist. The technologies described above should result in processed slices of semiconductor material; wherein the great majority of devices and internal connections are made by material processing. The terminals brought out of the packages will be functional in nature and relatively easy to work with. The inherently low cost and high reliability of Integrated Equipment Components should, along with the elimination of complexity and specialized "character of . . . ," result in electronics pervading our entire social structure.

Table 3. Generations of Electronics

Generation	Basic Product	Limitations of Electronics
First	Tubes	Cost
Second	Transistors	Reliability
Third	Integrated Circuits	Complexity
Fourth	Integrated Components Equipment	Specialized Character of . . .

Fourth Generation of Electronics

Because of the dramatic nature of large scale integrated electronics it seems appropriate to define it as the fourth generation of electronics. Table 3 suggests that the first generation of electronics, namely tubes, made a major contribution because it was possible to manufacture them at relatively low cost. This opened up the radio market in the 1920's and 30's and was the beginning of electronics.

The transistor can be identified as defining the second generation of electronics. Reliability was its principal early contribution, with low cost soon following. A key aspect of the transistor is that it is fabricated by materials processing rather than by the mechanical techniques used to build vacuum tubes.

Integrated circuits identified a third generation of electronics; here materials processing has been expanded to where complete circuits are fabricated on a chip of silicon. Another mechanical operation, namely that of connecting together discrete devices into circuits, has been eliminated.

As we move into the fourth generation of electronics, namely that of Integrated Equipment Components (IEC's), it is clear that a key technological result will be the use of materials processing in place of the mechanical operations of interconnecting thousands of circuits. This will result in IEC's which are easy to use and should result in electronics becoming truly pervasive.

Structure of the Electronics Industry

Such a radical change in the technological base of electronics can be expected to have a dramatic impact on the structure of the electronics industry. Figure 24 shows the author's view as to what will happen to the electronics industry.

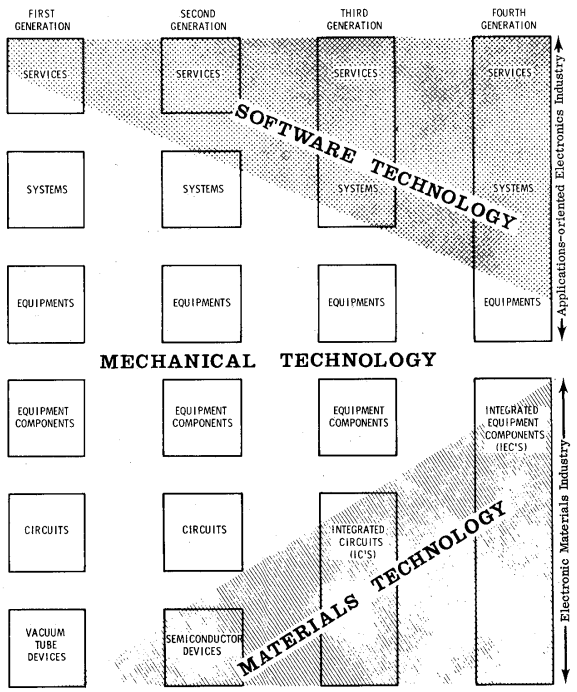


Figure 24. Structure of electronics industry.

This figure forecasts that expansion of materials technology to the IEC level will result in the integration of the device, circuit, and equipment businesses into a single business . . . segment. Those companies which will make up this business segment will integrate from materials up through equipment components. In order to do this, those companies must provide not only for materials technology, but also for device, circuit, and equipment design and fabrication capabilities. Because of the magnitude of this total problem, it seems likely that four or five large integrated [9] electronics suppliers will provide "electronic material," i.e., IEC's, IC's and devices on a very broad base to a much larger applications-oriented electronics industry.

Because of the tremendous expansion of the use of electronics which will result from the overcoming of the four limitations of electronics discussed above, the applications side of the electronics industry will expand in an unprecedented manner. While making this expansion, we forecast in Fig. 24 that much more emphasis will be given to the "software" aspect of electronics by this applications-oriented industry. By software we do not mean simply programming, but rather use the term in the broad sense where the customers' total problem is considered and solved.

The applications-oriented companies will use IEC's and other peripheral equipment components to provide a total solution to a customer's problem. It can be expected that this will be a very broad and diverse business consisting of many companies, a number of which are relatively small and specialize in a particular area of application. The materials-based integrated equipment component companies will relate to these applications-oriented companies much the same way as the chemical industry provides processed chemicals to a very large applications-oriented industry such as the clothing industry.

Another possible structure of the electronics industry is one that is highly integrated vertically such that systems houses provide their own IEC's. While this may happen to some degree, it is forecast that a very large materials-based integrated electronics business will still develop which supplies IEC's, IC's and devices on a very broad base to industry. The principal reason for this is the very pervasiveness that electronics will achieve. Compared to the very large number of companies which will use electronics, only relatively few companies will find it profitable to fabricate their own IEC's. Those companies whose internal requirements make it profitable for them to supply a part of their own IEC requirements will also depend upon the IEC suppliers for a significant part of their requirements. The sheer size of their needs, which is what makes it profitable for them to operate an internal facility, is also what makes it impossible for an internal operation to satisfy all of their needs.

Finally, it is forecast that the IEC suppliers will vertically integrate in selected areas of equipments, systems and services. For example, the author's own company has interest in providing geophysical equipment, systems and services to the oil and related industries. Such vertical integration will be a small fraction of the total application area of electronics.

It is concluded that the expansion of materials technology to the level where Integrated Equipment Components are achieved on slices of semiconductor will result in an electronics industry consisting of two major segments, one based on materials technology, the other based on software technology. Materials technology will provide the technological base for a concentrated Integrated Electronics industry which will supply IEC's, IC's and devices on a very broad base to a much larger application-oriented electronics

industry whose principal technology is software. Vertical integration will occur selectively, but will have no major effect on the overall division of the industry into these two major segments.

ACKNOWLEDGMENTS

The author is indebted to his colleagues at Texas Instruments for many stimulating discussions and helpful work on the subject of LSI: in particular, to Jay Lathrop for discussions of the overall aspect of the technology of LSI; to Jack Kilby for his personal leadership of the discretionary wiring approach to LSI; to Ray Warner for the forecasts and insight into the MOS technology.

With respect to more general aspects of LSI, discussions with Richard J. Hanschen, Cecil Dotson, Willis Adcock and Jack Kilby have been most helpful. And finally, the farsighted vision of Patrick E. Haggerty on the pervasiveness and general impact of Integrated Electronics has provided stimulus to the author's thinking.

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